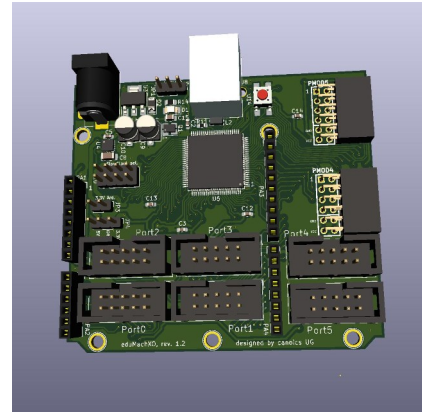


eduMachXO FPGA board

Features

- Lattice MachXO 2280 FPGA device (LCMXO2280C-3TN100)
- USB programmable (onboard FTDI USB-to-serial-converter)
- 6x 10-pin low profile header connectors (5V-TTL)
- 2x 12-pin Digilent™ PMOD connectors (3.3V-LVTTL)
- Arduino™ Uno compatible connectors
- power supply via USB-bus (5V) or external connector (7-12V)
- high-efficiency DC/DC buck converter for 3.3V generation
- 12 MHz system clock
- slow clock available via onboard divider (Jumper configurable)
- low-active button for e.g. reset



Power configuration

The power configuration is defined by three Jumpers JP1, JP3 and JP4.

Jumper	Configuration	Description
JP1	1-1-0 Jack	external power via DC-Jack with 7-12V
	0-1-1 Bus-powered	USB-bus-powered
	0-0-0 Arduino	5V Arduino connector
JP3	0-0	Arduino 3.3V pin is not supplied from the board's power regulator
	1-1 supply 3.3V	Arduino 3.3V pin is supplied from the board's power regulator
JP4	0-0-0 IOREF= pin	IOREF is supplied by the IOREF of the Arduino connector (shield/slave mode) or by pin 2 of a 10-pin low profile header
	0-1-1 IOREF=3.3V	IOREF is 3.3V from the board's power regulator (master mode)
	1-1-0 IOREF=5V	IOREF is 5V (master mode)

Clock Configuration

The eduMachXO-Board contains an on-board MEMS-Oscillator running on 12 MHz. The system clock and divided variants are supplied to the FPGA.

MachXO pin	Frequency	Description
39	PB10F	12 MHz System clock
87	PT9B	1.43 Hz 2.86 Hz 22.89 Hz 91.55 Hz Frequency depends on the placement of Jumper J10 (<i>Attention: only one connection is allowed!</i>)

Port mapping

General purpose ports / connectors

In order to connect peripherals to the board, several connectors are provided.

MachXO pin		Port Name
67 ... 69, 71 ... 75	PR8C, PR8B, PR8A, PR5D, PR4B, PR5A, PR3B, PR3A	Port 0
89, 92, 93, 95 ... 99	PT8E, PT6D, PT6F, PT4B, PT4A, PT3B, PT2B, PT2A	Port 1
54, 55, 57, 58, 60 ... 63	PR17B, PR17A, PR15B, PR15A, PR13B, PR13A, PR11B, PR11A	Port 2
77 ... 79, 81, 82, 84 ... 86	PT15C, PT14B, PT14A, PT12D, PT12C, PT11B, PT11A, PT10B	Port 3
4, 5, 7, 8, 10 ... 13	PL3D, PL4B, PL7A, PL7B, PL9C, PL9D, PL10C, PL10D	Port 4, PMOD4
14 ... 16, 18, 19, 21 ... 23	PL11C, PL13A, PL13B, PL14D, PL14C, PL16C, PL17A, PL17B	Port 5, PMOD5

Arduino connectors

Nr.	Power PA1	"Analog" PA2	Digital PA3	Digital PA4
1	NC	Port0[0] = 75 (PR3A), SCL	Port0[0] = 75 (PR3A), SCL	Port1[7] = 89 (PT8E)
2	IOREF, <i>see JP4</i>	Port0[1] = 74 (PR3B), SDA	Port0[1] = 74 (PR3B), SDA	Port1[6] = 92 (PT6D)
3	Port0[6] = 68 (PR8B), Reset	Port0[2] = 73 (PR5A)	NC (AREF)	Port1[5] = 93 (PT6F)
4	3.3V, <i>see JP3</i>	Port0[3] = 72 (PR5B)	GND	Port1[4] = 95 (PT4B)
5	5V, <i>see JP1</i>	Port0[4] = 71 (PR5D)	Port3[2] = 84 (PT11B), SCK	Port1[3] = 96 (PT4A)
6	GND	Port0[5] = 69 (PR8A)	Port3[3] = 82 (PT12C), MISO	Port1[2] = 97 (PT3B)
7	GND	-	Port3[4] = 81 (PT12D), MOSI	Port1[1] = 98 (PT2B), TX
8	Vin, <i>DC-Jack input</i>	-	Port3[5] = 79 (PT14A), SSEL	Port1[0] = 99 (PT2A), RX
9	-	-	Port3[6] = 78 (PT14B)	-
10	-	-	Port3[7] = 77 (PT15C)	-

Additional peripherals

MachXO pin	Function	Description
32	PB2C	reset button Pressed: logical "0" (low-active) Released: logical "1"

USB RS232/UART interface channel

The FTDI USB interface chip is able to provide a second COM port channel (or a SPI- or JTAG-interface in conjunction with FTDI's D2XX driver). Please note, that for SPI or JTAG usage the EEPROM of the FTDI-chip has to be configured/modified accordingly.

MachXO pin		Wire (RS232), Bridge-IC names		Wire (SPI)	Wire (JTAG)
53	PR18A	TxD	(FPGA: in)	SK (FPGA:in)	TCK
52	PR18B	RxD	(FPGA: out)	DO (FPGA:in)	TDI
51	PR19B	RTS	(FPGA: in)	DI (FPGA: out)	TDO
49	PB16	CTS	(FPGA: out)	CS (FPAG: in)	TMS
65	PR10A	DTR	(FPGA: in)	GPIOL0	GPIOL0
64	PR10B	DSR	(FPGA: out)	GPIOL1	GPIOL1

Special Pins

MachXO pin		Function	Description
8	PL7B	GSRN (Port4[4])	This FPGA-pin is dedicated to be programmed as a low-active global system-reset.
19	PL14C	TSALL (Port5[3])	This pin is routed in the FPGA as a "tristate all output signals". For using this functionality, use the TSALL software primitive.

Revision History

Rev 0.9a	2018/01/30	initial version
Rev 1.0	2018/07/09	first production version for GHSE
Rev. 1.1	2018/12/07	IOREF made selectable, DTR and DSR connected
Rev. 1.2	2019/10/20	improve EMC on USB bus, 2 nd production version

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Appendix: Schematic

